REMARKS

Claims 1-38 are pending and rejected by the examiner. Claims 1, 8 and 32 are independent claims.

The examiner rejected claims 1-38 under 35 U.S.C. §112, second paragraph, as being indefinite.

Applicant has amended claims 1, 8 and 32. The claims, as amended, avoid the use of vague and indefinite language, and clearly define applicant's invention. For example, claim 1, as amended, recites "an out-of-order microinstruction pointer (μIP) stack for storing pointers in a microcode (μcode) execution core, the pointers placed on the out-of order microinstruction pointer stack and removed from the microinstruction pointer stack before it is known if a sequence of microinstructions pointed to by the pointers is valid." Applicant's claim clearly defines the out-of-order microinstruction pointer stack that contains pointers placed on the out-of order microinstruction pointer stack and removed from the microinstruction pointer stack before it is known if a sequence of microinstructions pointed to by the pointers is valid.

The examiner uses Gage to reject claims 1, 3, 4, 8, 10, 11, 15-22 and 26-38 as having been anticipated.

Claims 1, 8 and 32, as amended, recite "an out-of-order microinstruction pointer (μIP) stack for storing pointers in a microcode (μcode) execution core, the pointers placed on the out-of order microinstruction pointer stack and removed from the microinstruction pointer stack before it is known if a sequence of microinstructions pointed to by the pointers is valid," or similar language. Gage neither describes nor suggests the quoted claim feature. Gage only cares about whether the stack is allowed to be overwritten or not. More specifically, Gage discloses:

> **The last bit of each stack entry is the valid bit. It is this bit that prevents overwriting of the contents of the stack, which would otherwise have happened in stack location 2 when the instruction "310: call 500" was received by the stack 30 in the example given above. The valid bit is set when a call occurs and remains set when a return occurs. The valid bit is only cleared after the control for the return microinstruction has propagated down a silo 32 past trap time, as will be explained later. (col. 7, lines 59-67)**

Accordingly, claims 1, 8 and 32 are not anticipated by Gage.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed.

Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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